WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of electro-thermal conversion elements; and

a plurality of switching devices for flowing electric currents through said plural electro-thermal conversion elements,

wherein:

said electro-thermal conversion elements and said switching devices are integrated on a first conductive type semiconductor substrate;

each of said switching devices is insulated gate type field effect transistor that includes: a second conductive type first semiconductor region formed on one principal surface of said semiconductor substrate; a first conductive type second semiconductor region for providing a channel region, said second semiconductor region being formed to adjoin said first semiconductor region; a second conductive type source region formed on the surface side of said second semiconductor region; a second conductive type drain region formed on the surface side of said first semiconductor region; and gate electrodes formed on said channel region with a gate insulator film put between them; and

said second semiconductor region comprises a

semiconductor having a impurity concentration higher than that of said first semiconductor region, said second semiconductor region being disposed between said drain regions arranged side by side.

2. A semiconductor device according to claim 1, wherein said second semiconductor region is formed adjacently to said semiconductor substrate.

3. A semiconductor device according to claim 1 or 2, wherein said source region and said drain region are disposed alternately in traverse directions.

4. A semiconductor device according to claim 1 or 2, wherein said electro-thermal conversion elements are connected with said drain region.

5. A semiconductor device according to claim 1 or 2, wherein two of said gate electrodes are formed with said source region put between them.

6. A semiconductor device according to claim 1 or 2, wherein an arrangement direction of said plural electro-thermal conversion elements and an arrangement direction of said plural switching

devices are in parallel.

7. A semiconductor device according to claim 1 or 2, wherein said drain regions of at least two of said insulated gate type field effect transistors are connected with one of said electro-thermal conversion elements, and said source regions of said plural insulated gate type field effect transistors are commonly connected.

8. A semiconductor device according to claim 1 or 2, wherein effective channel lengths of said insulated gate type field effect transistors are determined on a difference of transversal diffusion quantities between in said second semiconductor region and in said source region.

9. A semiconductor device according to claim 1 or 2, wherein said insulated gate type field effect transistors severally comprise a first conductive type diffusion layer for pulling out an electrode such that said diffusion layer penetrates said source region.

10. A semiconductor device according to claim 1 or 2, wherein drain sides of said gate electrodes are formed on insulator films thicker

than said gate insulator film.

11. A semiconductor device according to claim 1 or 2, wherein drain sides of said gate electrodes are formed on field insulator films.

12. A semiconductor device according to claim 1 or 2, wherein said first semiconductor region is a well formed by introduce of a reverse conductive type impurity from a surface of said semiconductor substrate.

13. A semiconductor device according to claim 1 or 2, wherein said first semiconductor region is composed of a plurality of wells formed by introduce of a reverse conductive type impurity from a surface of said semiconductor substrate and by transversal separation at every drain region.

14. A semiconductor device according to claim 1 or 2, wherein said second semiconductor region includes a lower region and a higher region in which its impurity concentration is higher than that in the lower region.

15. A semiconductor device according to claim 1 or 2, wherein said drain region is disposed

separately from drain side end portions of said gate electrodes.

16. A semiconductor device according to claim 1 or 2, wherein said source region overlaps said gate electrodes.

17. A semiconductor device according to claim 1 or 2, wherein:

said drain sides of said gate electrodes are formed on insulator films thicker than said gate insulator film, and

said drain region aligns itself end portions of thicker insulator films.

18. A semiconductor device according to claim 1 or 2, wherein said second semiconductor region, said source region and said drain region have sectional structures symmetrical on its right side and on its left side, said structures being formed by introduce of impurities by oblique ion implantation.

19. A semiconductor device according to claim 1 or 2, wherein said semiconductor substrate is an OFF substrate.

20. A semiconductor device according to claim 1 or 2, wherein liquid exhaust portions corresponding to said electro-thermal conversion elements are formed.

21. A semiconductor device according to claim 1 or 2, wherein said electro-thermal conversion elements are made of thin film resistance elements.

22. A method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of switching devices for flowing electric currents through said plural electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing

said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer.

23. A method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of switching devices for flowing electric currents through said plural electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a field insulator film on said semiconductor layer selectively;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film and said field insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer by utilizing said field insulator film as a mask.

24. A method according to claim 22 or 23, further comprising the steps of:

performing a first conductive type ion implantation into at least a channel region put between said source region and said semiconductor layer on the surface side of said semiconductor region through said gate electrode after said step of forming said semiconductor region; and

performing a heat treatment for activating the implanted impurity electrically.

25. A method according to claim 22 or 23, further comprising the steps of:

performing a first conductive type ion implantation into at least a channel region put between said source region and said semiconductor layer on the surface side of said semiconductor

region through said gate electrode after said step of forming said semiconductor region; and

performing a heat treatment for activating the implanted impurity electrically,

wherein said ion implantation is ion implantation in which ions of boron are implanted in energy of 100 keV or more.

26. A method according to claim 22 or 23, wherein:

at least two of said drain regions of MIS type field effect transistors being switching devices are connected with one of said electro-thermal conversion elements, and

said sources of said plural MIS type field effect transistors are commonly connected.

27. A method for manufacturing a semiconductor device, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer,

wherein said method can obtain a transistor structure symmetrical to said source region.

28. A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation obliquely to said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

29. A method according to claim 27, wherein said step of forming said second conductive type source region includes a step of performing ion implantation obliquely to said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

30. A method according to claim 27, wherein said step of forming said second conductive type drain region includes a step of performing ion implantation obliquely to said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

31. A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

32. A method according to claim 27, wherein said step of forming said second conductive type source region includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

33. A method according to claim 27, wherein said step of forming said second conductive type drain region includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

34. A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation of boron in high energy of 100 keV or more.

35. A method for manufacturing a semiconductor device in which a plurality of insulated gate type field effect transistors are arranged in an array, said method comprising the steps of:

forming a second conductive type first semiconductor region on one principal surface of a first conductive type semiconductor substrate;

forming a gate insulator film on said first semiconductor region;

forming a plurality of gate electrodes on said gate insulator film;

forming a first conductive type second semiconductor region by diffusing a first conductive type impurity after implanting the impurity between adjoining two of said gate electrodes by using said two gate electrodes as masks at a fixed angle to a normal line direction of said semiconductor substrate while rotating said semiconductor substrate; and

forming a second conductive type source

region in said second semiconductor region by utilizing said two gate electrodes as masks and a second conductive type drain region severally in two of said first semiconductor regions disposed to put said second semiconductor region between them by implanting the impurity at the fixed angle to the normal line direction of said semiconductor substrate while rotating said semiconductor substrate.

36. A method for manufacturing a semiconductor device in which a plurality of insulated gate type field effect transistors are arranged in an array, said method comprising the steps of:

forming a second conductive type first semiconductor region on one principal surface of a first conductive type semiconductor substrate;

forming a field insulator film selectively on said first semiconductor region;

forming a gate insulator film on said first semiconductor region;

forming gate electrodes on said gate insulator film and said field insulator film;

forming a first conductive type second semiconductor region by diffusing a first conductive type impurity after implanting the

impurity between two of said gate electrodes by using said two gate electrodes as masks at a fixed angle to a normal line direction of said semiconductor substrate while rotating said semiconductor substrate; and

forming a second conductive type source region in said second semiconductor region by utilizing said two gate electrodes as masks and a second conductive type drain region severally in two of said first semiconductor regions disposed to put said second semiconductor region between them by utilizing said field insulator film as a mask by implanting the impurity at the fixed angle to the normal line direction of said semiconductor substrate while rotating said semiconductor substrate.

37. A method according to claim 35 or 36, wherein said second semiconductor region is formed deeper than said first semiconductor region.

38. A method according to claim 35 or 36, wherein a heating resistance element connected with said drain region electrically is formed.

39. A method for manufacturing a semiconductor device, said method comprising the

steps of:

forming a second conductive type first semiconductor region on a first conductive type semiconductor substrate including one principal surface having a plane direction inclining against a lower dimensional plane direction;

forming a gate insulator film in said first semiconductor region;

forming a gate electrode on said gate insulator film;

forming a second semiconductor region by diffusing a first conductive type impurity after performing ion implantation of the impurity into said semiconductor substrate perpendicularly by utilizing said gate electrode as a mask; and

forming a second conductive type source region in said second semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region in said second semiconductor region by performing ion implantation of impurities severally perpendicularly to said semiconductor substrate.

40. A method for manufacturing a semiconductor device, said method comprising the steps of:

forming a second conductive type first

semiconductor layer on a first conductive type semiconductor substrate including one principal surface having a plane direction inclining against a lower dimensional plane direction;

forming a field insulator film in said first semiconductor region selectively;

forming a gate insulator film in said first semiconductor region;

forming a gate electrode on said gate insulator film and said field insulator film;

forming a second semiconductor region by diffusing a first conductive type impurity after performing ion implantation of the impurity into said semiconductor substrate perpendicularly by utilizing said gate electrode as a mask; and

forming a second conductive type source region in said second semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region in said second conductive type second semiconductor region by utilizing said field insulator film as a mask by performing ion implantation of impurities severally perpendicularly to said semiconductor substrate.

41. A method according to claim 39 or 40, wherein said plane direction of said principal

surface of said semiconductor substrate inclines to said lower dimensional plane direction at a degree of a range from 3° to 10°.

42. A method according to claim 39 or 40, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100) plane at a degree of a range from 3° to 10°.

43. A method according to claim 39 or 40, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100) plane at an angle of 4°.

44. A method according to claim 39 or 40, wherein said step of forming said second semiconductor region diffuses said first conductive type impurity such that said impurity is deeper than said first semiconductor region.

45. A method according to claim 39 or 40, wherein a plurality of insulated gate type field effect transistor are arranged in an array.

46. A semiconductor device in which a plurality of insulated gate type field effect

transistors are disposed in an array, said insulated gate type field effect transistors severally comprising:

a second conductive type first semiconductor region formed on a first conductive type semiconductor substrate including one principal surface having a plane direction inclining to a lower dimensional plane direction;

a first conductive type second semiconductor region formed to separate said first semiconductor region, said second semiconductor region having a concentration higher than that of said first semiconductor region;

a second conductive type source region formed in said second semiconductor region; and

a second conductive type drain region formed in said first semiconductor region.

47. A device according to claim 46, wherein said plane direction of said principal surface of said semiconductor substrate inclines to said lower dimensional plane direction at a degree of a range from 3° to 10°.

48. A device according to claim 46, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100)

plane at a degree of a range from 3° to 10°.

49. A device according to claim 46, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100) plane at an angle of 4°.

50. A device according to claim 46, wherein depth of said second semiconductor region is deeper than that of said first semiconductor region.

51. A liquid jet apparatus comprising:

a semiconductor device including liquid exhaust portions corresponding to electro-thermal conversion elements, said semiconductor device according to any one of claims 1, 2 and 46;

a liquid container for containing liquid jetted from said liquid exhaust portions by means of said electro-thermal conversion elements; and

a controller for supplying a drive controlling signal for driving insulated gate type field effect transistors in said semiconductor device.